Alveo Data Center Accelerator Card Platforms

User Guide

UG1120 (v1.5) July 30, 2021

Revision History

The following table shows the revision history for this document.

Section	Revision Summary
07/30/2021 Version 1.5	

Chapter 5: Alveo Platforms	Updated information about available platforms.
	• **Added:**
	  • U50 Gen3x16 NoDMA base_1 Platform
	  • U200 Gen3x16 XDMA base_1 Platform

All platforms	Where present, changed *Timestamp* to *Platform UUID* and *Interface UUID*, which better correspond to values in XRT.
04/23/2021 Version 1.4	
Chapter 5: Alveo Platforms	Updated available platforms. • **Added:** U250 Gen3x16 XDMA 2_1 Platform
Chapter 4: Platform Features	Slave-bridge (SB) feature renamed to host memory (HM). • **Added:** Gigabit Transceiver (GT) • **Updated:** Slave-bridge (SB) renamed to host memory (HM).
Chapter 5: Alveo Platforms	Under *Tool Support*, removed 2021.2 column.
Alveo PCIe Information	Replaced content with link to Appendix A in the *Alveo Card Out-of-Band Management Specification for Server BMC* documentation, which provides the same information.
U250 Gen3x16 XDMA 3_1 Platform	Added target card: A-U250-P64G-PQ-G
	Updated the descriptions for OS Version, removing *as the opener to this block* from the first sentence: Only present for Ubuntu packages (as the opener to this block).
01/13/2021 Version 1.3	
Chapter 4: Platform Features	Two feature descriptions added: host memory transfers and dynamic function eXchange technology
Package Naming Convention 2020.1 Release and Later	Updated information for operating systems, where new packages will support all Ubuntu releases.

Chapter 5: Alveo Platforms	Updated available platforms.
	• **Removed:**
	  • U50 XDMA 201920_1 Platform
	  • U50 XDMA 201910_1 Platform
	  • U200 XDMA 201830_1 Platform
	  • U250 XDMA 201830_1 Platform
	  • U250 Gen3x16 XDMA 3_1 Platform
	  • U280 XDMA 201920_2 Platform
	  • U280 XDMA 201920_1 Platform
	  • U280 XDMA 201910_1 Platform
	• **Added:**
	  • U250 Gen3x16 XDMA 3_1 Platform

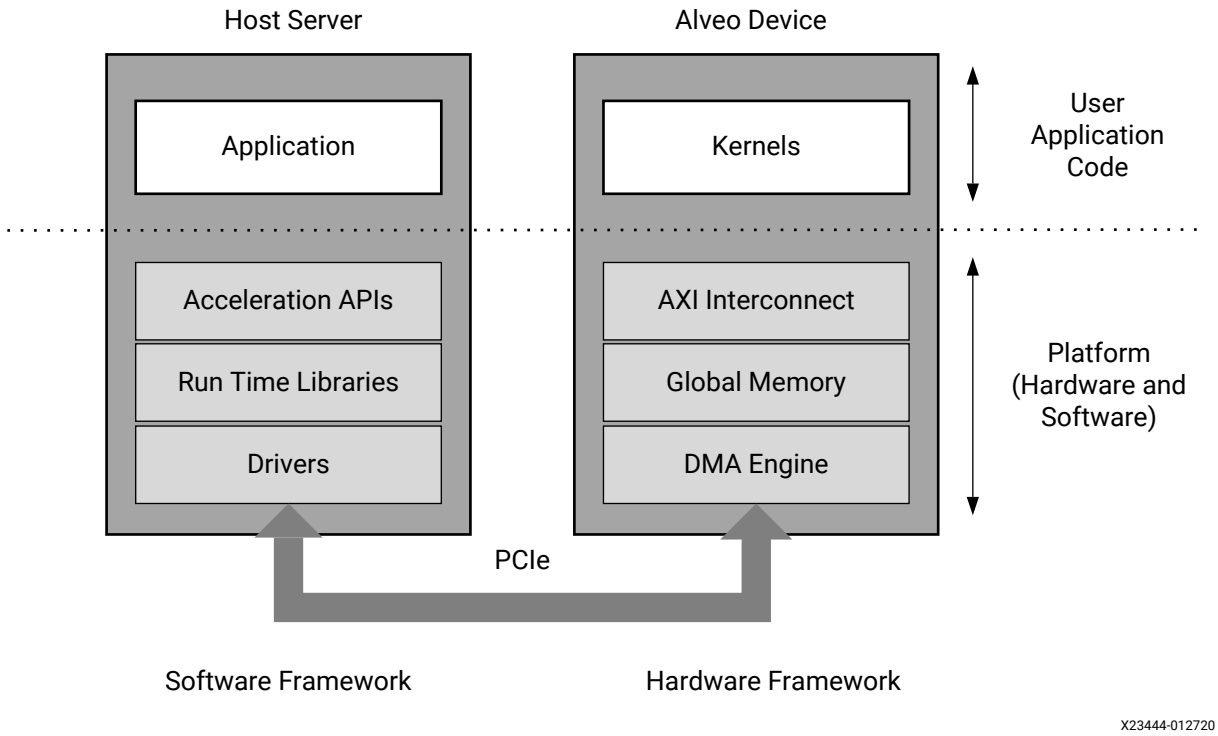
Section	Revision Summary
Alveo PCIe Information	New topic capturing PCIe information for Alveo U200, U250, U280, and U50 cards.
U50 Gen3x4 XDMA base_2 Platform	Updated values.
U50 Gen3x16 XDMA 201920_3 Platform	Updated values.
U200 XDMA 201830_2 Platform	Updated values.
U250 XDMA 201830_2 Platform	Updated values.
U250 Gen3x16 XDMA 3_1 Platform	Added platform.
U280 XDMA 201920_3 Platform	Updated card shutdown description with regard to the satellite controller. Updated values.
6/26/2020 Version 1.2	
Chapter 3: Platform Naming and Life Cycle	Updated section to delineate between the platform releases prior to 2020.1 and the 2020.1 release.
Chapter 5: Alveo Platforms	Updated release notes and target card information in each platform section.
U50 Gen3x4 XDMA base_2 Platform	Added platform information.
U50LV Gen3x4 XDMA base_2 Platform	Added platform information.
U50 Gen3x16 XDMA 201920_3 Platform	Added Vitis tools 2020.1 support.
U200 XDMA 201830_2 Platform	
U250 XDMA 201830_2 Platform	
U280 XDMA 201920_3 Platform	
4/22/2020 Version 1.1	
Table 8: xilinx_u50_gen3x16_xdma_201920_3 Platform Resource Availability Per SLR	Changed the title from xilinx_u50_xdma_201920_2 to xilinx_u50_gen3x16_xdma_201920_3.
Table 9: Available Memory Resources per SLR	Changed the platform name in Note 1 from xilinx_u50_xdma_201920_2 to xilinx_u50_gen3x16_xdma_201920_3.
Table 10: xilinx_u50_gen3x16_xdma_201920_3 Deployment Platform Installation Download Links	Changed the download links.
U50 XDMA 201920_1 Platform	Changed heading title from U50 XDMA 201920_2 Platform to U50 XDMA 201920_1 Platform.
U50 XDMA 201910_1 Platform	Changed heading title from U50 XDMA 201920_1 Platform to U50 XDMA 201910_1 Platform.
3/10/2020 Version 1.0.1	
General	Updated links throughout document.
2/29/2020 Version 1.0	
Initial release.	The *Available Platforms* section removed from the *Vitis Unified Software Platform Documentation: Application Acceleration Development* (UG1393). Added the xilinx_u50_gen3x16_xdma_201920_3 and xilinx_u280_xdma_201920_3 platforms.

Table of Contents

Overview

Xilinx Alveo™ Data Center accelerator cards are PCI Express® compliant cards designed to accelerate compute-intensive applications such as machine learning, data analytics, and video processing in a server or workstation. The Vitis core development kit provides verified platforms defining all the required hardware and software interfaces (shown in gray in the following figure), allowing you to design custom acceleration applications (shown in white) that are easily integrated into the Vitis programming model.

Figure 1: **Platform Overview**

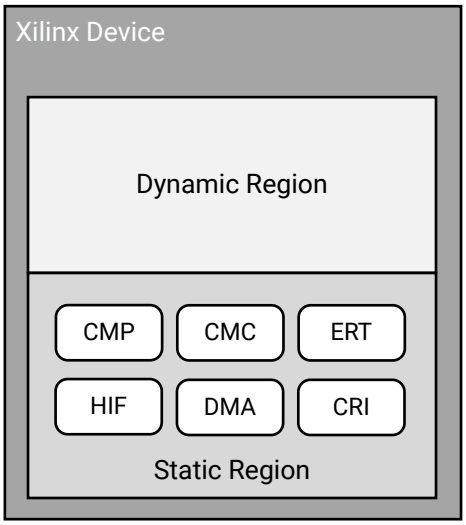


On the Xilinx device, a platform consists of a static region and a dynamic region. The static region of the platform provides the basic infrastructure for the card to communicate with the host and hardware support for the kernel. It includes the following features:

- **Host Interface (HIF):** PCIe endpoint to enable communication with external PCIe host
- **Direct Memory Access (DMA):** XDMA IP and AXI Protocol Firewall IP

- **Clock, Reset, and Isolation (CRI):** Basic clocking and reset for card bring-up and operation. Reset and Dynamic Function eXchange isolation structure are required for isolation during partial bitstream download.
- **Card Management Peripheral (CMP):** Peripherals responsible for board health and diagnostics, debug, and programming
- **Card Management Controller (CMC):** UART/I2C communication to satellite controller (MSP432), QSFP, sensors and manages firmware updates from the host (over PCIe)
- **Embedded RunTime Scheduler (ERT):** Schedule and monitor compute units during kernel execution

Figure 2: **Dynamic and Static Regions In a Platform**



Accelerated kernels go into the dynamic region. The features and resources available for accelerated kernels are described in Chapter 5: Alveo Platforms.

DMA Configurations

DMA Features

Xilinx provides a high-performance platform configuration to design custom acceleration applications with XDMA.

The XDMA platform, available on all Alveo accelerator cards provides:

- Memory-mapped DMA transfer
- High-bandwidth transfers
- Kernel support for memory-mapped AXI4

Table 1: **DMA Customization Features**

Feature	XDMA
Host interface	Gen3 x16 w/ 512-bit data path
Data path	512-bit wide memory-mapped AXI4
DMA transactions	Memory-mapped transfers between on card DDR4/PLRAM memories
Maximum transfer size	256 MB
DDR4 channels	U200/U250: 4x DDR4 16 GB (64 GB maximum) U280: 2x DDR4 16 GB

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Chapter 3

Platform Naming and Life Cycle

Package Naming Convention 2020.1 Release and Later

Starting with the 2020.1 release, Alveo platforms are delivered through three types of Linux installation packages outlined in the following table.

Table 2: **Platform Installation Package Types**

Package	Description
Partition	Contains a device bitstream that implements part of the deployment platform in the Alveo card.
Validate	Contains code to validate a platform installation and Alveo card setup.
Firmware	Contains compiled SC and CMC firmware binary files.

The following section describes the package naming convention for partition and validate types. They differ slightly from firmware.

Partition and Validate Package Naming

The partition and validate installation package names are generated by concatenating the following elements:

```
<name>_<version>-<release>-<architecture>[-<OS version>].<extension>
```

Each element consists of one or more sub-elements and are further described in the following table.

Table 3: **Partition and Validate Package Element Fields**

Element	Sub-element	Description	Examples
Name	Company	Vendor name	xilinx
	Card	Card name	u50 u250
	Chassis	Connectivity to the server	gen3x16-xdma gen3x4-xdma
	Partition	Partition name distinguishes the partition type and can be one of base, shell or validate.	base shell validate
Version	Iteration(s)	Version of chassis. Dot separated list of one or more integers. Increments when the corresponding chassis interface changes.	2 1.1
Release	Release	Integer release number.	2200000
Architecture	Architecture	Indicates the architecture the package is built for. noarch – No Architecture all	noarch all
OS Version	OS Version	Only present for Ubuntu packages (as the opener to this block). Indicates supported Ubuntu version for some packages. New packages will support all Ubuntu releases and are denoted as *all*.	16.04 18.04 all
Extension	Extension	Package file extension	RPM DEB

The following is an example of a deployment installation package for Ubuntu 16.04.

```
xilinx-u50-gen3x4-xdma-base_2-2200000_all_16.04.deb
```

Once a deployment partition package is installed, you can use XRT commands to display the partition installed on the card. See xbmgmt Utility in the Application Acceleration Development flow of the *Vitis Unified Software Platform Documentation* (UG1416).

Because the version number indicates compatibility with other partitions, the release number is not displayed. The following is the displayed partition name for the example package.

```
xilinx_u50_gen3x4_xdma_base_2
```

Firmware Package Naming

Firmware (SC and CMC) installation package names are generated by concatenating the following elements:

```
<name>-<version>-<release>-<architecture>[-<OS version>].<extension>
```

Each element consists of one or more sub-elements as listed in the following table.

Table 4: **Firmware Package Element Fields**

Element	Sub-element	Description	Examples
Name	Company	Vendor name	`xilinx`
	Product	Firmware product name	`cmc` `sc-fw`
	Card	Card name	u250 u50
Version	Version	Firmware version number. Three integers joined by dots.	1.0.13 4.3.9
Release	Release	CMC firmware uses an integer. SC firmware uses an alpha-numeric number separated with a dot.	2500000 1.a9fc625
Architecture	Architecture	Indicates the architecture the package is built for. noarch – No Architecture all	noarch all
OS Version	OS Version	Only present for Ubuntu packages. Indicates the supported Ubuntu version for some packages. New packages will support all Ubuntu releases and are denoted as *all*.	16.04 18.04 all
Extension	Extension	Package file extension	RPM DEB

The following are examples of `cmc` and `sc-fw` package names:

```
xilinx-cmc-u50_1.0.20-2853996_all_16.04.deb
```

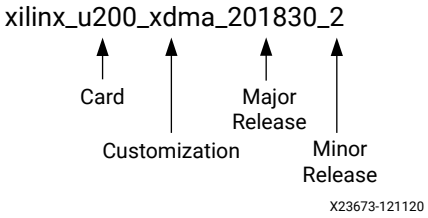
```
xilinx-sc-fw-u50-5.0.27-2.e289be9_16.04.deb
```

Platform Naming Convention Prior to 2020.1

Platforms are delivered via standard RPM and DEB Linux installation packages. The package name adheres to the nomenclature described in the following figure and provides the target card name, any customized configurations, the major release version, and the minor release versions.

For example, a platform for the U200 card with a main customization level XDMA that was built using the 2018.3 release might have a package name of `xilinx_u200_xdma_201830_2`.

Figure 3: **Example of Package Name**



Package Naming Conventions

Package names include the following information:
`<company>_<card>_<customization>_<major_release>_<minor_release>`

- **Company:** Xilinx
- **Card:** Series name of the card.
- **Customization:** Significant platform feature set. In this case, `XDMA` is the available customization.
- **Major Release:** Includes new features or capabilities. The six-digit number represents the Vitis tool release (version) used to build the platform. The platform can work across multiple major XRT and Vitis releases.
- **Minor Release:** Includes bug fixes and minor updates. Appends the major release with another number.

> **RECOMMENDED:** *Whenever possible, update to the latest release of a platform.*

Life-cycle of a Platform

Platforms have at least one year of backward compatibility with XRT, but not more than two. If IP used in the dynamic region of the platform is auto-upgraded for the same time frame, then generally:

- A platform generated from a release that has major revision of tools/run time such as 2019.1 is backward compatible until the last release of 2020 (2020.2).
- A platform generated from a release that has minor revision of tools/run time such as 2019.2 is also backward compatible until the last release of 2020 (2020.2).

Note: Xilinx reserves the right to make a backward *incompatible* change once a year with a major revision of XRT, a platform, or the Vitis core development kit. Major revision changes are usually done in the first release of a calendar year.

Platform Features

Different platform releases can include one or more of the following features. Features use resources in the static region of the platform.

Chapter 5: Alveo Platforms lists the features supported by each platform.

Table 5: **Feature Types**

Feature	Description
P2P	Shorthand for PCIe® peer-to-peer communication. Enables direct DMA transfer of data between two Alveo cards via the PCIe bus without temporarily buffering data within the host DDR memory. Without this feature the host CPU and memory are used for card-to-card communication. For more information, see XRT documentation on PCIe Peer-to-Peer (P2P).
M2M	Enabling on-card data transfers between card memory resources. Platforms that do not support this feature only transfer memory through host CPU and memory. For more information, see XRT documentation on Memory-to-Memory (M2M) support.
HM	Shorthand for PCIe host memory transfers. The AXI subordinate interface allows the card FPGA to directly read and write to host memory, bypassing the DMA. For more information, see XRT documentation on PCIe host memory.
DFX	Dynamic function eXchange (DFX) technology allows the card to change functionality on the fly *without* power-cycling the server, which enables some platforms to reconfigure DMA links. Current platforms come in one of two DFX variants. • **DFX-1RP:** The PCIe core and the DMA engine are combined and reside in the static region of the platform. These are also known as one stage platforms. • **DFX-2RP:** The PCIe core resides in the static region of the FPGA (also known as the base) while the DMA engine is dynamically loaded into a new reconfiguration region used by the shell partition. These are also known as two stage platforms. For more information, see Dynamic Function Exchange in XRT Documentation.
GT	Shorthand for Gigabit Transceiver (GT) kernel connection. This platform allows for transceiver connection of user-provided MAC within an RTL-kernel for in-line QSFP networking access.

Alveo Platforms

This section outlines the accelerator cards for data centers and the available target platforms. A target platform provides the firmware for the accelerator card running in a specific configuration. A target platform must be installed with Xilinx Runtime (XRT).

There can be more than one target platform for a given card. Each platform indicates the customization, release name, available features, and tool support. The following sections contain specific details on each available platform. The following table lists the available target platforms per Alveo data center card.

RECOMMENDED: *Only the following target platforms are supported. Any device or platform that is not listed is not supported. Xilinx recommends using the latest platform release.*

Table 6: **Available Alveo Platforms**

Card	Release Name	Features					Tool Support		
		P2P	M2M	HM	DFX	GT	2020.2	2021.1	2021.2
U50	U50 Gen3x16 NoDMA base_1 Platform	–	–	Yes	1RP	Yes			Yes
	U50 Gen3x4 XDMA base_2 Platform	–	–	–	1RP	Yes	Yes	Yes	Yes
	U50 Gen3x16 XDMA 201920_3 Platform	–	–	–	1RP	Yes	Yes	Yes	Yes
U50LV	U50LV Gen3x4 XDMA base_2 Platform	–	–	–	1RP	Yes	Yes	Yes	Yes
U200	U200 Gen3x16 XDMA base_1 Platform	Yes	Yes	Yes	1RP	Yes	Yes	Yes	Yes
	U200 XDMA 201830_2 Platform	Yes	Yes	–	1RP	–	Yes	Yes	Yes
U250	U250 Gen3x16 XDMA 3_1 Platform	Yes	Yes	Yes	2RP	Yes	Yes	Yes	Yes
	U250 Gen3x16 XDMA 2_1 Platform	Yes	Yes	Yes	2RP	Yes	Yes	Yes	Yes
	U250 XDMA 201830_2 Platform	Yes	–	–	1RP	–	Yes	Yes	Yes
U280	U280 XDMA 201920_3 Platform	Yes	–	–	1RP	Yes	Yes	Yes	Yes

Alveo PCIe Information

To view PCIe information for Alveo U200, U250, U280, and U50 cards, see Appendix A in the *Alveo Card Out-of-Band Management Specification for Server BMC* documentation.

U50 and U50LV

The following platforms and the voltages they support are listed in this section.

- U50 supports V_{NORM} where V_{CCINT} = 0.85V
- U50LV supports V_{LOW} where V_{CCINT} = 0.72V

The complete technical specifications are available in the *Alveo U50 Data Center Accelerator Cards Data Sheet* (DS965).

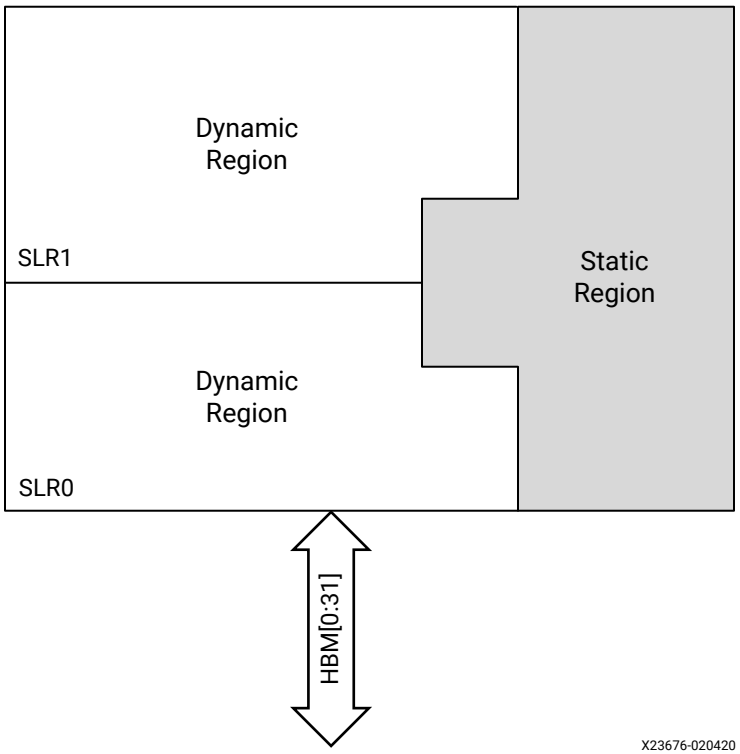
U50 Gen3x16 XDMA 201920_3 Platform

- **Platform name:** xilinx_u50_gen3x16_xdma_201920_3
- **Supported by:** Vitis tools 2019.2 through 2021.1, with support planned through 2021
- **Platform UUID:** `F465B0A3-AE8C-64F6-19BC-150384ACE69B`
- **Interface UUID:** `862C7020-A250-293E-3203-6F19956669E5`
- **Release Date:** February 2020
- **Created by:** 2019.2 tools
- **Supported XRT versions:** 2019.2_PU2 through 2021.1, with support planned through 2021
- **Satellite controller (SC) FW release:** 5.0.27 updated to 5.1.7 with the November 2020 release
- **Link speed:** Gen3 x16
- **Target card:** A-U50-P00G-PQ-G

  For more information, see Alveo U50 Data Center Accelerator Card.
- **Release Notes:** Change log and known issues for the platform and the SC and CMC firmware are available in the *Alveo U50 Master Release Notes Answer Record* 75163.

The platform implements the device floorplan shown in the following figure and uses resources across the multiple super logic regions (SLR) of the device. The static and dynamic regions are shown across the SLRs, along with the available HBM memory connections associated with SLR0.

Figure 4: **Floorplan**



To get the same information for development platforms, after you install the Vitis design kit, use the `platforminfo` command utility. It reports information on interfaces, clocks, valid SLRs, allocated resources, and memory in a structured format. For more information, see platforminfo Utility in the Application Acceleration Development flow of the *Vitis Unified Software Platform Documentation* (UG1416).

Card Thermal and Electrical Protections

With the xilinx_u50_gen3x16_xdma_201920_3 platform, there are protections to ensure production cards operate within electrical and thermal limits while running acceleration kernels. The following table defines the power and thermal thresholds used to trigger each protection. These protections take three forms and are triggered when the respective thresholds are crossed:

- Clock throttling
- Clock shutdown
- Card shutdown

Clock throttling protection reduces the kernel clock frequencies when any sensor reaches or exceeds their respective clock throttling threshold as listed in the following table. It is a dynamic process that lowers the clock frequencies while power exceeds the associated threshold. By lowering the clock frequencies, clock throttling reduces the required power and subsequently generated heat. Only when all sensor values fall below their respective clock throttling threshold values will the application clocks be restored to full performance.

Clock shutdown shuts down the kernel clocks when any sensor reaches or exceeds their respective clock shutdown threshold given in the following table and will cause an AXI firewall trip that can crash the application on the host. Because the card ends up in an unknown state the XRT driver will issue a command to reset the card. It typically takes a couple minutes until the card is usable again.

Card shutdown removes power to the FPGA when any sensor reaches or exceeds their respective shutdown threshold and will pull the card off the PCIe bus. Power to the SC will remain on. No AXI firewall trip will be issued. A cold reboot of the server is required to recover. The shutdown thresholds listed in the following table are higher than the clock shutdown thresholds and protect the card from damage.

TIP: *Review the Linux `dmesg` command output to determine if a protection was activated. An example of the clock shut down messaging is shown:*

```
[ 777.531353] clock.m clock.m.23068673: dev ffff97a9e5c3c810,
clock_status_check: Critical temperature or power event, kernel clocks
have been stopped, run 'xbutil valiate -q' to continue. See AR 73398
for more details.
```

Table 7: **Thermal and Electrical Protection Thresholds**

Sensor Description	Clock Throttling Threshold	Clock Shutdown Threshold	Shutdown Threshold
12V PEX power	62W	65W	N/A
3V3 PEX power	9.9W	11W	N/A
V_{CCINT} current	56,000 mA	N/A	60,000 mA
V_{CCINT} temperature	N/A	110°C	125°C
Maximum temperature of device and HBM	92°C	97°C	107°C
QSFP temperature	N/A	85°C[1]	90°C[1]

Notes:

1. Refer to QSFP module data sheet.

Clocking

The platform provides a 300 MHz default clock to run the accelerator.

Available Resources After Platform Installation

The following table lists the available resources in the dynamic region of each SLR. It represents the total device resources after subtracting those used by the static region.

Table 8: **xilinx_u50_gen3x16_xdma_201920_3 Platform Resource Availability Per SLR**

Resource	SLR0	SLR1
CLB LUT	369K	362K
CLB register	738K	724K
Block RAM tile	564	564
UltraRAM	304	304
DSP	2580	2760

Memory

The Alveo U50 card has 8 GB of high-bandwidth memory (HBM) accessible through 32 pseudo channels. In addition, it is possible to use the device logic resources for small, fast, on-chip memory accesses as PLRAM. The following table lists the allocation of memory resources per SLR.

Table 9: **Available Memory Resources per SLR**

Resources	SLR0	SLR1
PLRAM memory channels (system port name)	PLRAM[0:1] (128K, block RAM)	PLRAM[2:3] (128K, block RAM)
HBM memory channels (system port name)	HBM [0:31] (8 GB)[1]	No connections

Notes:

1. The xilinx_u50_gen3x16_xdma_201920_3 platform allows the use of 28 (maximum) of the 32 available HBM pseudo channels. Using more will generate errors during hardware build. Xilinx recommends using pseudo-channels 0:27.

Deployment Platform Installation

To run applications with this platform, download the deployment installation packages corresponding to your OS listed in the following table. Then, use the installation procedures described in *Alveo U50 Data Center Accelerator Card Installation Guide* (UG1370).

Table 10: **xilinx_u50_gen3x16_xdma_201920_3 Deployment Platform Installation Download Links**

OS	Download Link
Ubuntu	https://www.xilinx.com/bin/public/openDownload?filename=xilinx-u50-gen3x16-xdma-all_1-2784799.deb.tar.gz
RedHat/CentOS	https://www.xilinx.com/bin/public/openDownload?filename=xilinx-u50-gen3x16-xdma-noarch_1-2784799.rpm.tar.gz

Accelerated applications have software dependencies. Work with your accelerated application provider to determine which XRT version to install.

Development Platform Installation

For developing applications for use with the Alveo Data Center Accelerator cards you must install and use the Vitis software platform. To set up an accelerator card for use in the development environment, follow the installation steps in:

- Installing Data Center Platforms in the *Vitis Unified Software Platform Documentation* (UG1416)
- Installing Xilinx Runtime in the *Vitis Unified Software Platform Documentation* (UG1416)

U50 Gen3x16 NoDMA base_1 Platform

- **Platform name:** xilinx_u50_gen3x16_nodma_base_1
- **Platform UUID:** `4429B71A-27E2-5E65-E708-E17D6FF2DF93`
- **Interface UUID:** `B56495F8-1F2A-0E27-FF1F-ABFDC441D260`
- **Release Date:** June 2021
- **Created by:** 2020.2 tools
- **Supported XRT versions:** 2021.1 with support planned through 2021
- **Satellite controller (SC) FW release:** Released with SC 5.2.6
- **Link speed:** Gen3 x16
- **Target card:** A-U50-P00G-PQ-G

  For more information, see Alveo U50 Data Center Accelerator Card.
- **Release Notes:** Change log and known issues for the platform and the SC and CMC firmware are available in the *Alveo U50 Master Release Notes Answer Record* 75163.

The xilinx_u50_gen3x16_nodma_base_1 is an application-specific platform. It provides direct access to host memory requiring the user logic for data movement. This platform requires pre-allocation of host memory. For more information, refer to https://xilinx.github.io/XRT/master/html/hm.html.

U50 Gen3x4 XDMA base_2 Platform

- **Platform name:** xilinx_u50_gen3x4_xdma_base_2
- **Platform UUID:** `447C677D-83C3-FFCA-029E-19DE0CC7D7E9`
- **Interface UUID:** `4CDA0BA9-AB64-B59C-535A-DADF2E0B1930`

- **Release Date:** June 2020
- **Created by:** 2020.1 tools
- **Supported XRT versions:** 2020.1 through 2021.1, with support planned through 2021
- **Satellite controller (SC) FW release:** 5.0.27 updated to 5.1.7 with the November 2020 release
- **Link speed:** Gen3 x4
- **Target card:** A-U50-P00G-PQ-G

  For more information, see Alveo U50 Data Center Accelerator Card.
- **Release Notes:** Change log and known issues for the platform and the SC and CMC firmware are available in the *Alveo U50 Master Release Notes Answer Record* 75163.

The xilinx_u50_gen3x4_xdma_base_2 is an application specific platform used with machine learning and video transcode application solutions. An application solution combines the platform and application into a single solution. Because application specific platforms are only used with an application, no Vitis development platform is provided.

U50LV Gen3x4 XDMA base_2 Platform

- **Platform name:** xilinx_u50lv_gen3x4_xdma_base_2
- **Platform UUID:** `CA1BD561-0169-A52C-E463-B3300DF98172`
- **Interface UUID:** `05A5E9D4-E079-740E-76C7-499FEEC81DB3`
- **Release Date:** June 2020
- **Created by:** 2020.1 tools
- **Supported XRT versions:** 2020.1 through 2020.2, with support planned through 2021
- **Satellite controller (SC) FW release:** 5.0.27 updated to 5.1.7 with the November 2020 release
- **Link speed:** Gen3 x4
- **Target card:** A-U50-P00G-LV-G

  For more information, see Alveo U50 Data Center Accelerator Card.
- **Release Notes:** Change log and known issues for the platform and the SC and CMC firmware are available in the *Alveo U50 Master Release Notes Answer Record* 75163.

The xilinx_u50lv_gen3x4_xdma_202010_1 is an application specific platform used with machine learning and video transcode application solutions. An application solution combines the platform and application into a single solution. Because application specific platforms are only used with an application, no Vitis development platform is provided.

U200

U200 Gen3x16 XDMA base_1 Platform

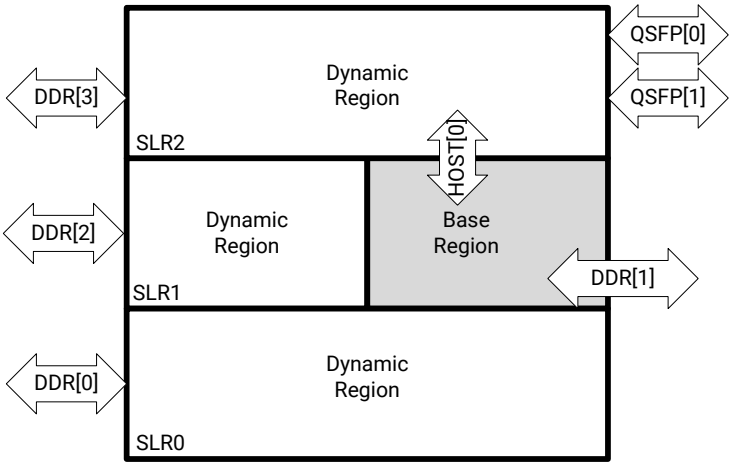
- **Platform name:** xilinx_u200_gen3x16_xdma_base_1
- **Supported by:**
  - Vitis 2021.1 tools with support planned through 2021
- **Platform UUID:** `A2D4F3CF-5B7A-0B7B-70F9-DA589CB5B3CD`
- **Interface UUID:** `15FB8DA1-F552-A9F9-23DE-6DC54AA8968F`
- **Release Date:** June 2021
- **Created by:** 2020.2 tools

- **Supported XRT versions:** 2021.1 with support planned through 2021
- **Satellite controller (SC) FW release:** 4.6.11
- **Link speed:** PCIe Gen3 x16
- **Target cards:**
  - A-U200-A64G-PQ-G

  For more information, see Alveo U200 Data Center Accelerator Card.
- **Release Notes:** Change log and known issues for the platform and the SC and CMC firmware are available in the *Alveo U200 Master Release Notes Answer Record* 75172.

The platform implements the device floorplan shown in the following figure and uses resources across the multiple super logic regions (SLR) of the device. The static and dynamic regions are shown across the FPGA SLRs, along with the available DDR memory connections associated with each SLR.

Figure 5: **Floorplan**



To get the same information for development platforms, after you install the Vitis design kit, use the `platforminfo` command utility. It reports information on interfaces, clocks, valid SLRs, allocated resources, and memory in a structured format. For more information, see platforminfo Utility in the Application Acceleration Development flow of the *Vitis Unified Software Platform Documentation* (UG1416).

Clocking

The platform provides a 300 MHz default clock to run the accelerator.

Available Resources After Platform Installation

The following table lists the available resources in the dynamic region of each SLR. It represents the total device resources after subtracting those used by the static region.

Table 11: **xilinx_u200_gen3x16_xdma_1_1 Platform Resource Availability Per SLR**

Resource	SLR 0	SLR 1	SLR 2
CLB LUT	385K	200K	383K
CLB register	771K	399K	765K
Block RAM tile	720	360	720
URAM	320	160	320
DSP	2280	1320	2280

Memory

The Alveo U200 card has a total of four available DDR memory banks. All but DDR[1] are located in the dynamic region. In addition, it is possible to use the device logic resources for small, fast, on-chip memory accesses as PLRAM. The following table lists the allocation of memory resources per SLR.

***Note*:** For details on assigning kernels to DDR memory channels, see Kernel SLR and DDR Memory Assignments in the Application Acceleration Development flow of the *Vitis Unified Software Platform Documentation* (UG1416).

Table 12: **Available Memory Resources per SLR**

Resources	SLR 0	SLR 1	SLR 2
DDR memory channels (system port name)	DDR[0] (16 GB DDR4)	DDR[1] (16 GB DDR4, static region) DDR[2] (16 GB DDR4, dynamic area)	DDR[3] (16 GB DDR4)
PLRAM memory channels (system port name)	PLRAM[0] (128K, Block RAM)	PLRAM[1] (128K Block RAM)	PLRAM[2] (128K Block RAM)
Host memory channels (system port name)			HOST[0] 16 GB on host

Deployment Platform Installation

To run applications with this platform, download the deployment installation packages corresponding to your OS listed in the following table. Then, use the installation procedures described in *Getting Started with Alveo Data Center Accelerator Cards* (UG1301).

Table 13: **xilinx_u200_gen3x16_xdma_1_1 Deployment Platform Installation Download Links**

OS	Download Link
Ubuntu	https://www.xilinx.com/bin/public/openDownload?filename=xilinx-u200-gen3x16-xdma-all_1-3209015.deb_2.tar.gz
Redhat/CentOS	https://www.xilinx.com/bin/public/openDownload?filename=xilinx-u200-gen3x16-xdma-noarch_1-3209015.rpm_2.tar.gz

Accelerated applications have software dependencies. Work with your accelerated application provider to determine which XRT version to install.

Development Platform Installation

For developing applications for use with the Alveo Data Center Accelerator cards you must install and use the Vitis software platform. To set up an accelerator card for use in the development environment, follow the installation steps in:

- Installing Data Center Platforms in the *Vitis Unified Software Platform Documentation* (UG1416)
- Installing Xilinx Runtime in the *Vitis Unified Software Platform Documentation* (UG1416)

U200 XDMA 201830_2 Platform

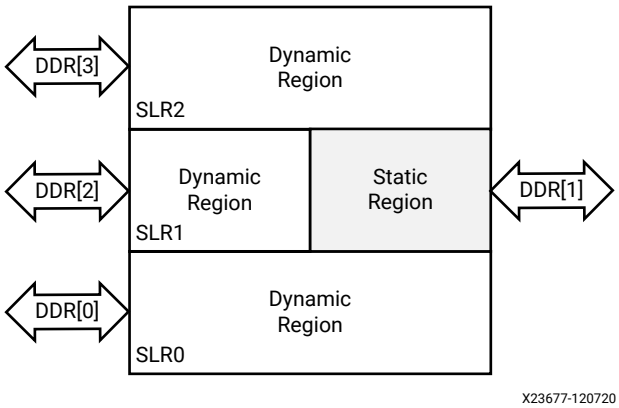
- **Platform name:** xilinx_u200_xdma_201830_2
- **Supported by:**
  - SDx 2018.3 through 2019.1
  - Vitis tools 2019.2 through 2021.1, with support planned through 2021
- **Platform ID:** `0x000000005d1211e8`
- **Release Date:** July 2019
- **Created by:** 2018.3 tools
- **Supported XRT versions:** 2018.3 through 2021.1, with support planned through 2021
- **Satellite controller (SC) FW release:** 4.2.0
- **Link speed:** Gen3 x16
- **Target cards:**
  - A-U200-A64G-PQ-G
  - A-U200-P64G-PQ-G

  For more information, see Alveo U200 Data Center Accelerator Card.

- **Release Notes:** Change log and known issues for the platform and the SC and CMC firmware are available in the *Alveo U200 Master Release Notes Answer Record* 75172.

The platform implements the device floorplan shown in the following figure and uses resources across the multiple super logic regions (SLR) of the device. The static and dynamic regions are shown across the FPGA SLRs, along with the available DDR memory connections associated with each SLR.

Figure 6: **Floorplan**



To get the same information for development platforms, after you install the Vitis design kit, use the `platforminfo` command utility. It reports information on interfaces, clocks, valid SLRs, allocated resources, and memory in a structured format. For more information, see platforminfo Utility in the Application Acceleration Development flow of the *Vitis Unified Software Platform Documentation* (UG1416).

Clocking

The platform provides a 300 MHz default clock to run the accelerator.

Available Resources After Platform Installation

The following table lists the available resources in the dynamic region of each SLR. It represents the total device resources after subtracting those used by the static region.

Table 14: **xilinx_u200_xdma_201830_2 Platform Resource Availability Per SLR**

Resource	SLR 0	SLR 1	SLR 2
CLB LUT	355K	160K	355K
CLB register	723K	331K	723K
Block RAM tile	638	326	638
URAM	320	160	320
DSP	2265	1317	2265

Memory

The Alveo U200 card has a total of four available DDR memory banks. All but DDR[1] are located in the dynamic region. In addition, it is possible to use the device logic resources for small, fast, on-chip memory accesses as PLRAM. The following table lists the allocation of memory resources per SLR.

Note: For details on assigning kernels to DDR memory channels, see Kernel SLR and DDR Memory Assignments in the Application Acceleration Development flow of the *Vitis Unified Software Platform Documentation* (UG1416).

Table 15: **Available Memory Resources per SLR**

Resources	SLR 0	SLR 1	SLR 2
DDR memory channels (system port name)	DDR[0] (16 GB DDR4)	DDR[1] (16 GB DDR4, static region) DDR[2] (16 GB DDR4, dynamic area)	DDR[3] (16 GB DDR4)
PLRAM memory channels (system port name)	PLRAM[0] (128K, Block RAM)	PLRAM[1] (128K Block RAM)	PLRAM[2] (128K Block RAM)

Deployment Platform Installation

To run applications with this platform, download the deployment installation packages corresponding to your OS listed in the following table. Then, use the installation procedures described in *Getting Started with Alveo Data Center Accelerator Cards* (UG1301).

Table 16: **xilinx_u200_xdma_201830_2 Deployment Platform Installation Download Links**

OS	Download Link
Ubuntu 18.04	https://www.xilinx.com/bin/public/openDownload?filename=xilinx-u200-xdma-201830.2-2580015_18.04.deb
Ubuntu 16.04	https://www.xilinx.com/bin/public/openDownload?filename=xilinx-u200-xdma-201830.2-2580015_16.04.deb
Redhat/CentOS	https://www.xilinx.com/bin/public/openDownload?filename=xilinx-u200-xdma-201830.2-2580015.x86_64.rpm

Accelerated applications have software dependencies. Work with your accelerated application provider to determine which XRT version to install.

Development Platform Installation

For developing applications for use with the Alveo Data Center Accelerator cards you must install and use the Vitis software platform. To set up an accelerator card for use in the development environment, follow the installation steps in:

- Installing Data Center Platforms in the *Vitis Unified Software Platform Documentation* (UG1416)

- Installing Xilinx Runtime in the *Vitis Unified Software Platform Documentation* (UG1416)

U250

U250 Gen3x16 XDMA 3_1 Platform

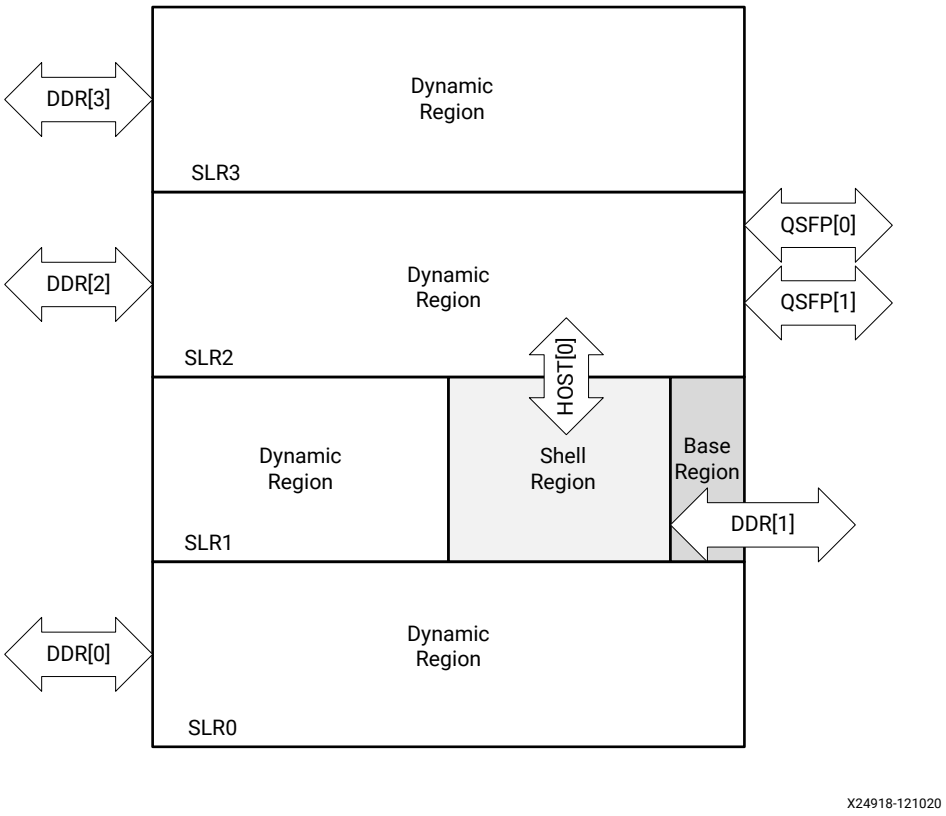
- **Platform name:** xilinx_u250_gen3x16_xdma_3_1
- **Supported by:**
  - Vitis tools 2020.2 to 2021.1, with support planned through 2021
- **Logic UUID:** `BD5FB8AB-AB26-6C32-6591-8257B5048E88`
- **Interface UUID:** `F2F6C5E1-273E-7894-8F2C-4806221462F2`
- **Release Date:** November 2020
- **Created by:** 2020.2 tools
- **Supported XRT versions:** 2020.2 to 2021.1, with support planned through 2021
- **Satellite controller (SC) FW release:** 4.6.6
- **Link speed:** Gen3 x16
- **Target cards:**
  - A-U250-A64G-PQ-G
  - A-U250-P64G-PQ-G

  For more information, see Alveo U250 Data Center Accelerator Card.
- **Release Notes:** Change log and known issues for the platform and the SC and CMC firmware are available in the *Alveo U250 Master Release Notes Answer Record* 75180.

Platform Details

The platform implements the device floorplan shown in the following figure and uses resources across the multiple super logic regions (SLR) of the device. The static and dynamic regions are shown across the SLRs, along with the available DDR memory connections associated with each SLR.

Figure 7: **Floorplan**



To get the same information for development platforms, if you install the Vitis design kit, use the `platforminfo` command utility. It reports information on interfaces, clocks, valid SLRs, allocated resources, and memory in a structured format. For more information, see platforminfo Utility in the Application Acceleration Development flow of the *Vitis Unified Software Platform Documentation* (UG1416).

***Note*:** Prior to running an application on DFX-2RP platforms, it is necessary to first program the shell partition. For more information, see 75975.

Clocking

The platform provides a 300 MHz default clock to run the accelerator.

Available Resources After Platform Installation

The following table lists the available resources in the dynamic region of each SLR. It represents the total device resources after subtracting those used by the static region.

Table 17: **xilinx_u250_gen3x16_xdma_3_1 Platform Resource Availability per SLR**

Resource	SLR 0	SLR 1	SLR 2	SLR 3
CLB LUT	420K	205K	407K	424K

Table 17: **xilinx_u250_gen3x16_xdma_3_1 Platform Resource Availability per SLR** *(cont'd)*

Resource	SLR 0	SLR 1	SLR 2	SLR 3
CLB register	839K	411K	815K	849K
Block RAM tile	668	384	660	672
URAM	312	128	308	320
DSP	3032	1536	2994	3072

Memory

The Alveo U250 card has a total of four available DDR memory banks. In addition, it is possible to use device logic resources for small, fast, on-chip memory accesses as PLRAM. The following table lists the allocation of memory resources per SLR.

***Note*:** For details on assigning kernels to DDR memory channels, see Kernel SLR and DDR Memory Assignments in the Application Acceleration Development flow of the *Vitis Unified Software Platform Documentation* (UG1416).

Table 18: **Available Memory Resources per SLR**

Resources	SLR 0	SLR 1	SLR 2	SLR3
DDR memory channels (system port name)	DDR[0] (16 GB DDR4)	DDR[1] (16 GB DDR4)	DDR[2] (16 GB DDR4)	DDR[3] (16 GB DDR4)
PLRAM memory channels (system port name)	PLRAM[0] (128K, Block RAM)	PLRAM[1] (128K Block RAM)	PLRAM[2] (128K Block RAM)	PLRAM[3] (128K Block RAM)
Host memory channels (system port name)	–	–	HOST[0] 16 GB on host	–

Deployment Platform Installation

To run applications with this platform, download the deployment installation packages corresponding to your OS listed in the following table. Then, use the installation procedures described in *Getting Started with Alveo Data Center Accelerator Cards* (UG1301).

***Note*:** Prior to running an application on DFX-2RP platforms, it is necessary to first program the shell partition. For more information, see 75975.

Table 19: **xilinx_u250_gen3x16_xdma_3_1 Deployment Platform Installation Download Links**

OS	Download Link
Ubuntu	https://www.xilinx.com/bin/public/openDownload?filename=xilinx-u250-gen3x16-xdma-platform_3.1-1_all.deb.tar.gz
RedHat/CentOS	https://www.xilinx.com/bin/public/openDownload?filename=xilinx-u250-gen3x16-xdma-platform-3.1-1.noarch.rpm.tar.gz

Accelerated applications have software dependencies. Work with your accelerated application provider to determine which XRT version to install.

Development Platform Installation

For developing applications for use with the Alveo Data Center Accelerator cards you must install and use the Vitis software platform. To set up an accelerator card for use in the development environment, follow the installation steps in:

- Installing Data Center Platforms in the *Vitis Unified Software Platform Documentation* (UG1416)
- Installing Xilinx Runtime in the *Vitis Unified Software Platform Documentation* (UG1416)

U250 Gen3x16 XDMA 2_1 Platform

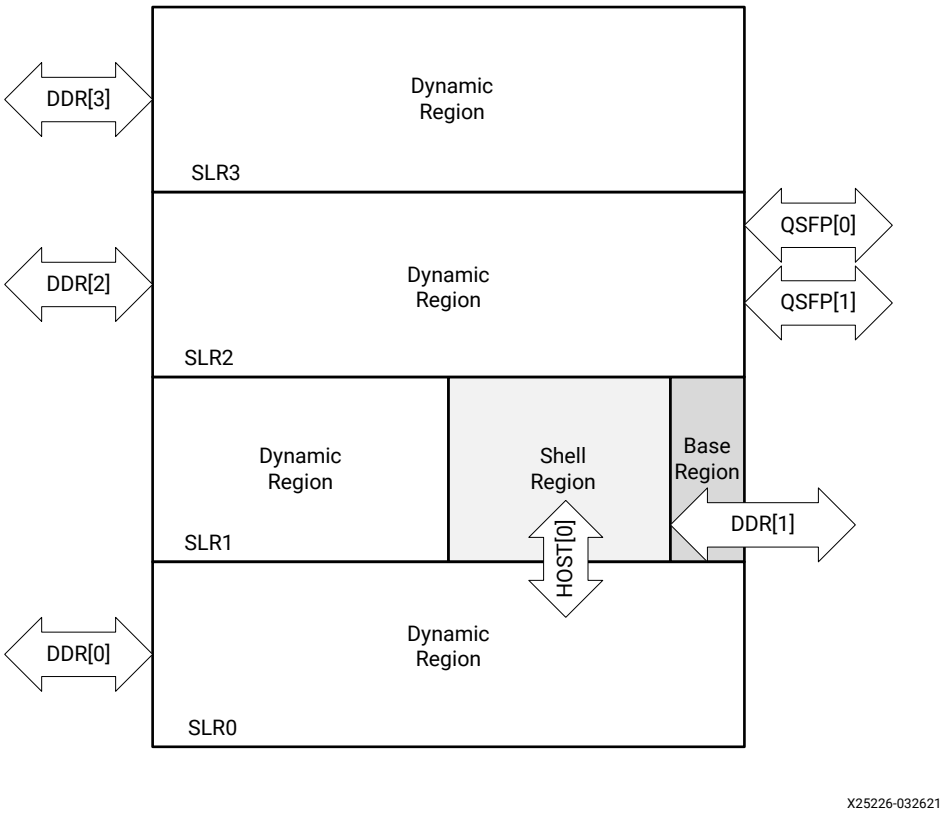
- **Platform name:** xilinx_u250_gen3x16_xdma_2_1
- **Supported by:** Vitis tools 2020.2
- **Logic UUID:** `C3AD6B03-7144-8CA9-494E-D5B672C7092A`
- **Interface UUID:** `13DB7987-A2D8-1BFF-743A-71ED8DF67C17`
- **Release Date:** April 2021
- **Created by:** 2020.1 tools
- **Supported XRT versions:** 202020.2.8.832
- **Satellite controller (SC) FW release:** 4.5.0
- **Link speed:** Gen3 x16
- **Target cards:**
  - A-U250-A64G-PQ-G
  - A-U250-P64G-PQ-G

  For more information, see Alveo U250 Data Center Accelerator Card.
- **Release Notes:** Change log and known issues for the platform and the SC and CMC firmware are available in the *Alveo U250 Master Release Notes Answer Record* 75180.

Platform Details

The platform implements the device floorplan shown in the following figure and uses resources across the multiple super logic regions (SLR) of the device. The static and dynamic regions are shown across the SLRs, along with the available DDR memory connections associated with each SLR.

Figure 8: **Floorplan**



To get the same information for development platforms, if you install the Vitis design kit, use the `platforminfo` command utility. It reports information on interfaces, clocks, valid SLRs, allocated resources, and memory in a structured format. For more information, see platforminfo Utility in the Application Acceleration Development flow of the *Vitis Unified Software Platform Documentation* (UG1416).

***Note*:** Prior to running an application on DFX-2RP platforms, it is necessary to first program the shell partition. For more information, see 75975.

Clocking

The platform provides a 300 MHz default clock to run the accelerator.

Available Resources After Platform Installation

The following table lists the available resources in the dynamic region of each SLR. It represents the total device resources after subtracting those used by the static region.

Table 20: **xilinx_u250_gen3x16_xdma_2_1 Platform Resource Availability per SLR**

Resource	SLR 0	SLR 1	SLR 2	SLR 3
CLB LUT	419K	205K	410K	424K

Table 20: **xilinx_u250_gen3x16_xdma_2_1 Platform Resource Availability per SLR** *(cont'd)*

Resource	SLR 0	SLR 1	SLR 2	SLR 3
CLB register	839K	410K	819K	848K
Block RAM tile	668	384	664	672
URAM	312	128	308	320
DSP	3032	1536	3016	3072

Memory

The Alveo U250 card has a total of four available DDR memory banks. In addition, it is possible to use device logic resources for small, fast, on-chip memory accesses as PLRAM. The following table lists the allocation of memory resources per SLR.

***Note*:** For details on assigning kernels to DDR memory channels, see Kernel SLR and DDR Memory Assignments in the Application Acceleration Development flow of the *Vitis Unified Software Platform Documentation* (UG1416).

Table 21: **Available Memory Resources per SLR**

Resources	SLR 0	SLR 1	SLR 2	SLR3
DDR memory channels (system port name)	DDR[0] (16 GB DDR4)	DDR[1] (16 GB DDR4)	DDR[2] (16 GB DDR4)	DDR[3] (16 GB DDR4)
PLRAM memory channels (system port name)	PLRAM[0] (128K, Block RAM)	PLRAM[1] (128K, Block RAM)	PLRAM[2] (128K, Block RAM)	PLRAM[3] (128K, Block RAM)
Host memory channels (system port name)	HOST[0] 16 GB on host	–	–	–

Deployment Platform Installation

To run applications with this platform, download the deployment installation packages corresponding to your OS listed in the following table. Then, use the installation procedures described in *Getting Started with Alveo Data Center Accelerator Cards* (UG1301).

***Note*:** Prior to running an application on DFX-2RP platforms, it is necessary to first program the shell partition. For more information, see 75975.

Table 22: **xilinx_u250_gen3x16_xdma_2_1 Deployment Platform Installation Download Links**

OS	Download Link
Ubuntu	https://www.xilinx.com/bin/public/openDownload?filename=xilinx-u250-gen3x16-xdma-platform-2.1-3_all_18.04.deb.tar.gz
RedHat/CentOS	https://www.xilinx.com/bin/public/openDownload?filename=xilinx-u250-gen3x16-xdma-platform-2.1-3.noarch.rpm.tar.gz

Accelerated applications have software dependencies. Work with your accelerated application provider to determine which XRT version to install.

Development Platform Installation

For developing applications for use with the Alveo Data Center Accelerator cards you must install and use the Vitis software platform. To set up an accelerator card for use in the development environment, follow the installation steps in:

- Installing Data Center Platforms in the *Vitis Unified Software Platform Documentation* (UG1416)
- Installing Xilinx Runtime in the *Vitis Unified Software Platform Documentation* (UG1416)

U250 XDMA 201830_2 Platform

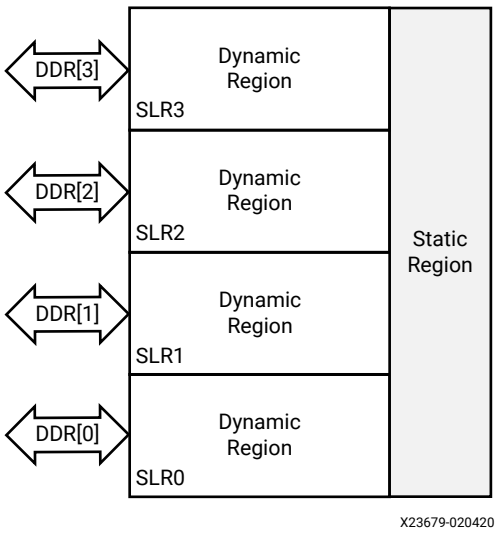
- **Platform name:** xilinx_u250_xdma_201830_2
- **Supported by:**
  - SDx 2018.3 through 2019.1
  - Vitis tools 2019.2 through 2021.1, with support planned through 2021
- **Platform ID:** `0x000000005d14fbe6`
- **Release Date:** July 2019
- **Created by:** 2018.3 tools
- **Supported XRT versions:** 2018.3 to 2021.1, with support planned through 2021
- **Satellite controller (SC) FW release:** 4.2.0
- **Link speed:** Gen3 x16
- **Target cards:**
  - A-U250-A64G-PQ-G
  - A-U250-P64G-PQ-G

  For more information, see Alveo U250 Data Center Accelerator Card.
- **Release Notes:** Change log and known issues for the platform and the SC and CMC firmware are available in the *Alveo U250 Master Release Notes Answer Record* 75180.

Platform Details

The platform implements the device floorplan shown in the following figure and uses resources across the multiple super logic regions (SLR) of the device. The static and dynamic regions are shown across the SLRs, along with the available DDR memory connections associated with each SLR.

Figure 9: **Floorplan**



To get the same information for development platforms, if you install the Vitis design kit, use the `platforminfo` command utility. It reports information on interfaces, clocks, valid SLRs, allocated resources, and memory in a structured format. For more information, see platforminfo Utility in the Application Acceleration Development flow of the *Vitis Unified Software Platform Documentation* (UG1416).

Clocking

The platform provides a 300 MHz default clock to run the accelerator.

Available Resources After Platform Installation

The following table lists the available resources in the dynamic region of each SLR. It represents the total device resources after subtracting those used by the static region.

Table 23: **xilinx_u250_xdma_201830_2 Platform Resource Availability per SLR**

Resource	SLR 0	SLR 1	SLR 2	SLR 3
CLB LUT	345K	345K	345K	345K
CLB register	705K	703K	703K	704K
Block RAM tile	500	500	500	500
URAM	320	320	320	320

Table 23: **xilinx_u250_xdma_201830_2 Platform Resource Availability per SLR** *(cont'd)*

Resource	SLR 0	SLR 1	SLR 2	SLR 3
DSP	2877	2877	2877	2877

Memory

The Alveo U250 card has a total of four available DDR memory banks. In addition, it is possible to use device logic resources for small, fast, on-chip memory accesses as PLRAM. The following table lists the allocation of memory resources per SLR.

***Note*:** For details on assigning kernels to DDR memory channels, see Kernel SLR and DDR Memory Assignments in the Application Acceleration Development flow of the *Vitis Unified Software Platform Documentation* (UG1416).

Table 24: **Available Memory Resources per SLR**

Resources	SLR 0	SLR 1	SLR 2	SLR3
DDR memory channels (system port name)	DDR[0] (16 GB DDR4)	DDR[1] (16 GB DDR4)	DDR[2] (16 GB DDR4)	DDR[3] (16 GB DDR4)
PLRAM memory channels (system port name)	PLRAM[0] (128K, Block RAM)	PLRAM[1] (128K Block RAM)	PLRAM[2] (128K Block RAM)	PLRAM[3] (128K Block RAM)

Deployment Platform Installation

To run applications with this platform, download the deployment installation packages corresponding to your OS listed in the following table. Then, use the installation procedures described in *Getting Started with Alveo Data Center Accelerator Cards* (UG1301).

Table 25: **xilinx_u250_xdma_201830_2 Deployment Platform Installation Download Links**

OS	Download Link
Ubuntu 18.04	https://www.xilinx.com/bin/public/openDownload?filename=xilinx-u250-xdma-201830.2-2580015_18.04.deb
Ubuntu 16.04	https://www.xilinx.com/bin/public/openDownload?filename=xilinx-u250-xdma-201830.2-2580015_16.04.deb
Redhat/CentOS	https://www.xilinx.com/bin/public/openDownload?filename=xilinx-u250-xdma-201830.2-2580015.x86_64.rpm

Accelerated applications have software dependencies. Work with your accelerated application provider to determine which XRT version to install.

Development Platform Installation

For developing applications for use with the Alveo Data Center Accelerator cards you must install and use the Vitis software platform. To set up an accelerator card for use in the development environment, follow the installation steps in:

- Installing Data Center Platforms in the *Vitis Unified Software Platform Documentation* (UG1416)
- Installing Xilinx Runtime in the *Vitis Unified Software Platform Documentation* (UG1416)

U280

U280 XDMA 201920_3 Platform

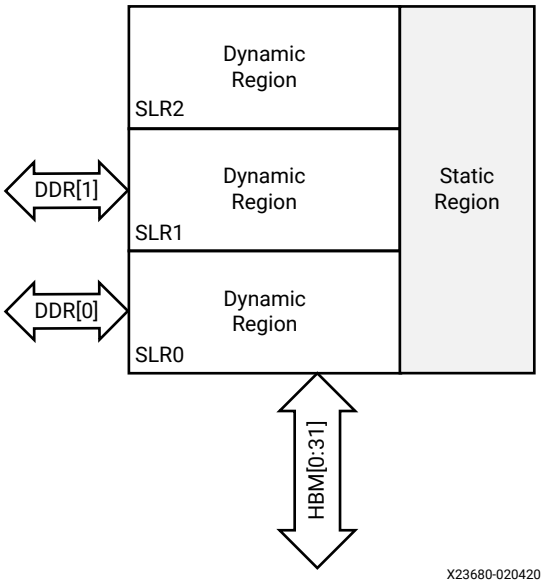
- **Platform name:** xilinx_u280_xdma_201920_3
- **Supported by:** Vitis tools 2019.2 through 2021.1, with support planned through 2021
- **Platform ID:** `0x5e278820`
- **Release Date:** February 2020
- **Created by:** 2019.2 tools
- **Supported XRT versions:** 2019.2_PU2 to 2021.1, with support planned through 2021
- **Satellite controller (SC) FW release:** 4.3.10
- **Link speed:** Gen3 x16
- **Target cards:**
  - A-U280-A32G-DEV-G
  - A-U280-P32G-PQ-G

  For more information, see Alveo U280 Data Center Accelerator Card.
- **Release Notes:** Change log and known issues for the platform and the SC and CMC firmware are available in the *Alveo U280 Master Release Notes Answer Record* 75183.

Platform Details

The platform implements the device floorplan shown in the following figure and uses resources across the multiple super logic regions (SLR) of the device. The static and dynamic regions are shown across the SLRs, along with the available DDR memory connections associated with each SLR.

Figure 10: **Floorplan**



To get the same information for development platforms, if you install the Vitis design kit, use the `platforminfo` command utility. It reports information on interfaces, clocks, valid SLRs, allocated resources, and memory in a structured format. For more information, see platforminfo Utility in the Application Acceleration Development flow of the *Vitis Unified Software Platform Documentation* (UG1416).

Clocking

The platform provides a 300 MHz default clock to run the accelerator.

Available Resources After Platform Installation

The following table lists the available resources in the dynamic region of each SLR. It represents the total device resources after subtracting those used by the static region.

Table 26: **xilinx_u280_xdma_201920_3 Platform Resource Availability per SLR**

Resource	SLR 0	SLR 1	SLR 2
CLB LUT	369K	333K	367K
CLB register	746K	675K	729K
Block RAM tile	507	468	512
URAM	320	320	320
DSP	2733	2877	2880

Memory

The Alveo U280 card has access to a total of 32 GB DDR memory and 8 GB HBM. The DDR memory banks are accessible through two memory controllers and the HBM is accessible through 32 pseudo channels. In addition, it is possible to use device logic resources for small, fast, on-chip memory accesses as PLRAM. The following table lists the allocation of memory resources per SLR.

***Note*:** For details on assigning kernels to DDR memory channels, see Kernel SLR and DDR Memory Assignments in the Application Acceleration Development flow of the *Vitis Unified Software Platform Documentation* (UG1416).

Table 27: **Available Memory Resources per SLR**

Resources	SLR 0	SLR 1	SLR 2
DDR memory channels (system port name)	DDR[0] (16 GB DDR4)	DDR[1] (16 GB DDR4)	No resources
HBM masters	HBM[0:31] (8 GB)	No resources	No resources
PLRAM memory channels (system port name)	PLRAM[0:1] (128K, Block RAM)	PLRAM[2:3] (128K, Block RAM)	PLRAM[4:5] (128K, Block RAM)

Deployment Platform Installation

To run applications with this platform, download the deployment installation packages corresponding to your OS listed in the following table. Then, use the installation procedures described in *Getting Started with Alveo Data Center Accelerator Cards* (UG1301).

Table 28: **xilinx_u280_xdma_201920_3 Deployment Platform Installation Download Links**

OS	Download Link
Ubuntu 18.04	https://www.xilinx.com/bin/public/openDownload?filename=xilinx-u280-xdma-201920.3-3246211_18.04.deb
Ubuntu 16.04	https://www.xilinx.com/bin/public/openDownload?filename=xilinx-u280-xdma-201920.3-3246211_18.04.deb
Redhat/CentOS	https://www.xilinx.com/bin/public/openDownload?filename=xilinx-u280-xdma-201920.3-3246211.x86_64.rpm

Accelerated applications have software dependencies. Work with your accelerated application provider to determine which XRT version to install.

Development Platform Installation

For developing applications for use with the Alveo Data Center Accelerator cards you must install and use the Vitis software platform. To set up an accelerator card for use in the development environment, follow the installation steps in:

- Installing Data Center Platforms in the *Vitis Unified Software Platform Documentation* (UG1416)

- Installing Xilinx Runtime in the *Vitis Unified Software Platform Documentation* (UG1416)

XILINX

Appendix A

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this guide:

U50

1. *Alveo U50 Data Center Accelerator Cards Data Sheet* (DS965)
2. *Alveo U50 Data Center Accelerator Card Installation Guide* (UG1370)
3. *Vitis Unified Software Platform Documentation* (UG1416)

U280

1. *Alveo U280 Data Center Accelerator Cards Data Sheet* (DS963)
2. *Getting Started with Alveo Data Center Accelerator Cards* (UG1301)
3. *Vitis Unified Software Platform Documentation* (UG1416)

U250

1. *Alveo U200 and U250 Data Center Accelerator Cards Data Sheet* (DS962)
2. *Getting Started with Alveo Data Center Accelerator Cards* (UG1301)
3. *Vitis Unified Software Platform Documentation* (UG1416)

U200

1. *Alveo U200 and U250 Data Center Accelerator Cards Data Sheet* (DS962)
2. *Getting Started with Alveo Data Center Accelerator Cards* (UG1301)
3. *Vitis Unified Software Platform Documentation* (UG1416)

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