

430-4593-AO

Dell® 430-4593 Compatible TAA Compliant 40GBase-SR4 QSFP+ Transceiver (MMF, 850nm, 150m, MPO, DOM)

Features

- SFF-8436 Compliance
- MPO Connector
- Commercial Temperature 0 to 70 Celsius
- Multi-mode Fiber
- Hot Pluggable
- Excellent ESD Protection
- Metal with Lower EMI
- RoHS Compliant and Lead Free



Applications

- 40GBase Ethernet
- Access and Enterprise

Product Description

This Dell® 430-4593 compatible QSFP+ transceiver provides 40GBase-SR4 throughput up to 150m over multi-mode fiber (MMF) using a wavelength of 850nm via an MPO connector. It is guaranteed to be 100% compatible with the equivalent Dell® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."



Absolute Maximum Ratings

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|----------------------------|--------|------|------|---------|------|
| Supply Voltage | Vcc | -0.3 | | 3.6 | V |
| Input Voltage | Vin | -0.3 | | Vcc+0.3 | V |
| Storage Temperature | Tst | -20 | | 85 | °C |
| Case Operating Temperature | Top | 0 | | 70 | °C |
| Humidity (non-condensing) | Rh | 5 | | 95 | % |

Recommended Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|----------------------------|--------|------|------|--------|------|
| Supply Voltage | Vcc | 3.13 | 3.3 | 3.47 | V |
| Operating Case Temperature | Tca | 0 | | 70 | °C |
| Data Rate Per Lane | fd | 2.5 | | 14.025 | Gbps |
| Humidity | Rh | 5 | | 85 | % |
| Power Dissipation | Pm | | | 1.5 | W |
| Fiber Bend Radius | Rb | 3 | | | cm |

Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---------------------------------------|--------|---------|------|------|-------|-------|
| Differential Input impedance | Zin | 90 | 100 | 110 | ohm | |
| Differential Output impedance | Zout | 90 | 100 | 110 | ohm | |
| Differential Input Voltage amplitude | ΔVin | 300 | | 1100 | mVp-p | |
| Differential output voltage amplitude | ΔVout | 500 | | 800 | mVp-p | |
| Skew | Sw | | | 300 | ps | |
| Bit Error Rate | BR | | | E-12 | | |
| Input Logic Level High | VIH | 2.0 | | VCC | V | |
| Input Logic Level Low | VIL | 0 | | 0.8 | V | |
| Output Logic Level High | VOH | VCC-0.5 | | VCC | V | |
| Output Logic Level Low | VOL | 0 | | 0.4 | V | |

Optical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|--|---|------|------|------|------|--------------------|
| Transmitter | | | | | | |
| Center Wavelength | λ_C | 840 | 850 | 860 | nm | |
| RMS Spectral Width | $\Delta\lambda$ | | | 0.65 | nm | |
| Average Optical Power per Channel | Pout | -7.5 | | 2.5 | dBm | |
| Difference in launch power between any two lanes (OMA) | | | | 4 | dB | |
| Extinction Ratio | ER | 3 | | | dB | |
| Peak power, each lane | | | | 4 | dBm | |
| Transmitter and dispersion penalty (TDP), each lane | TDP | | | 3.5 | dB | |
| Eye Mask Coordinates: X1, X2, X3, Y1, Y2, Y3 | Specification Values 0.23, 0.34, 0.43, 0.27, 0.35, 0.4 | | | | | Hit Ratio = 5x10-5 |
| Receiver | | | | | | |
| Center Wavelength | λ_C | 840 | 850 | 860 | nm | |
| Stressed receiver sensitivity in OMA, each lane | | | | -5.4 | dBm | 1 |
| Average power at receiver input, each lane | | -9.5 | | 2.4 | dBm | |
| Receiver Reflectance | | | | -12 | dB | |
| Peak power, each lane | | | | 4 | dBm | |
| LOS Assert | | -30 | | | dBm | |
| LOS De-Assert - OMA | | | | -7.5 | dBm | |
| LOS Hysteresis | | 0.5 | | | dB | |

Notes:

1. Measured with conformance test signal at TP3 for BER = 10e-12

Pin Descriptions

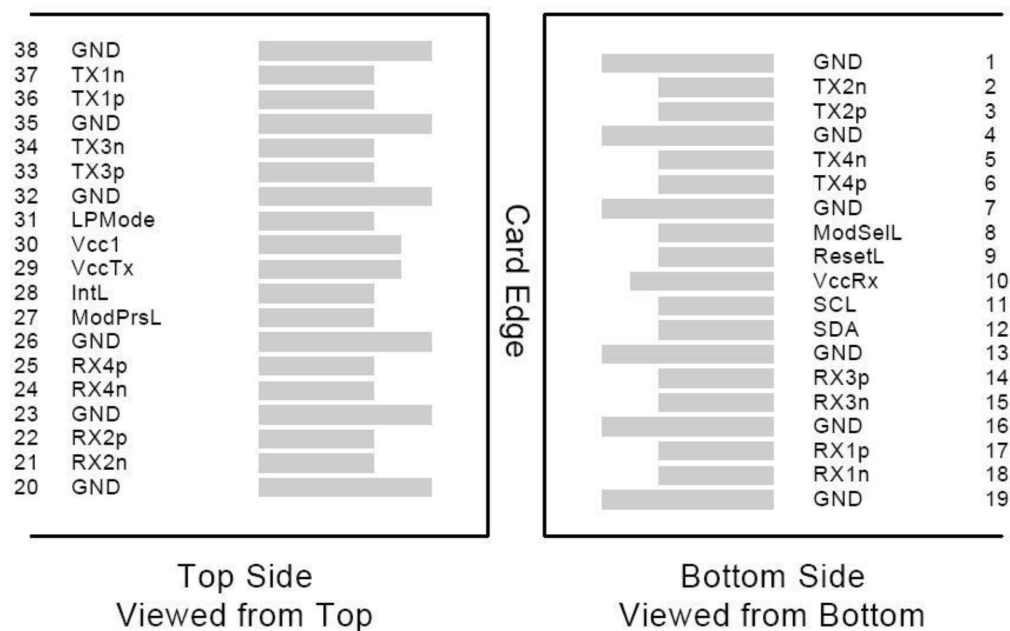
| Pin | Logic | Symbol | Name/Descriptions | Ref. |
|-----|-------------|-------------------|---|------|
| 1 | | GND | Module Ground | 1 |
| 2 | CML-I | Tx2- | Transmitter inverted data input | |
| 3 | CML-I | Tx2+ | Transmitter non-inverted data input | |
| 4 | | GND | Module Ground | 1 |
| 5 | CML-I | Tx4- | Transmitter inverted data input | |
| 6 | CML-I | Tx4+ | Transmitter non-inverted data input | |
| 7 | | GND | Module Ground | 1 |
| 8 | LVTTL-I | MODSEIL | Module Select | 2 |
| 9 | LVTTL-I | ResetL | Module Reset | 2 |
| 10 | | VCCR _x | +3.3v Receiver Power Supply | |
| 11 | LVC MOS-I | SCL | 2-wire Serial interface clock | 2 |
| 12 | LVC MOS-I/O | SDA | 2-wire Serial interface data | 2 |
| 13 | | GND | Module Ground | 1 |
| 14 | CML-O | RX3+ | Receiver non-inverted data output | |
| 15 | CML-O | RX3- | Receiver inverted data output | |
| 16 | | GND | Module Ground | 1 |
| 17 | CML-O | RX1+ | Receiver non-inverted data output | |
| 18 | CML-O | RX1- | Receiver inverted data output | |
| 19 | | GND | Module Ground | 1 |
| 20 | | GND | Module Ground | 1 |
| 21 | CML-O | RX2- | Receiver inverted data output | |
| 22 | CML-O | RX2+ | Receiver non-inverted data output | |
| 23 | | GND | Module Ground | 1 |
| 24 | CML-O | RX4- | Receiver inverted data output | |
| 25 | CML-O | RX4+ | Receiver non-inverted data output | |
| 26 | | GND | Module Ground | 1 |
| 27 | LVTTL-O | ModPrsL | Module Present, internal pulled down to GND | |
| 28 | LVTTL-O | IntL | Interrupt output, should be pulled up on host board | 2 |
| 29 | | VCCT _x | +3.3v Transmitter Power Supply | |
| 30 | | VCC1 | +3.3v Power Supply | |
| 31 | LVTTL-I | LPMode | Low Power Mode | 2 |
| 32 | | GND | Module Ground | 1 |
| 33 | CML-I | Tx3+ | Transmitter non-inverted data input | |

| | | | | |
|-----------|-------|------|-------------------------------------|---|
| 34 | CML-I | Tx3- | Transmitter inverted data input | |
| 35 | | GND | Module Ground | 1 |
| 36 | CML-I | Tx1+ | Transmitter non-inverted data input | |
| 37 | CML-I | Tx1- | Transmitter inverted data input | |
| 38 | | GND | Module Ground | 1 |

Notes:

1. Module circuit ground is isolated from module chassis ground with in the module.
2. Open collector; should be pulled up with 4.7k-10k ohms on host board to a voltage between 3.15V and 3.6V.

Electrical Pin-out Details



ModSel Pin

The ModSel is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSel allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSel is “High”, the module will not respond to any 2-wire interface communication from the host. ModSel has an internal pull-up in the module.

ResetL Pin

Reset. LPMoDe_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length ($t_{\text{Reset_init}}$) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_{init}) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_{init}) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMoDe Pin

Operate in the low power mode (less than 1.5 W power consumption) This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

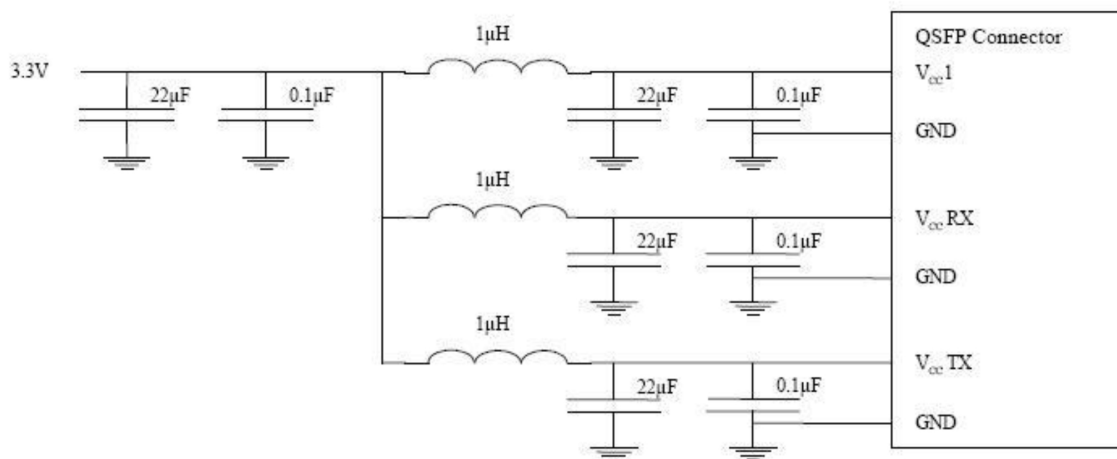
ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and de-asserted “High” when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

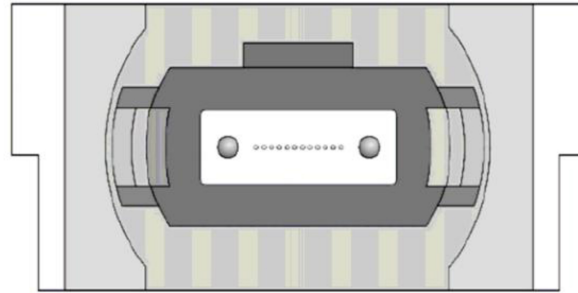
Power Supply Filtering

The host board should use the power supply filtering shown below.



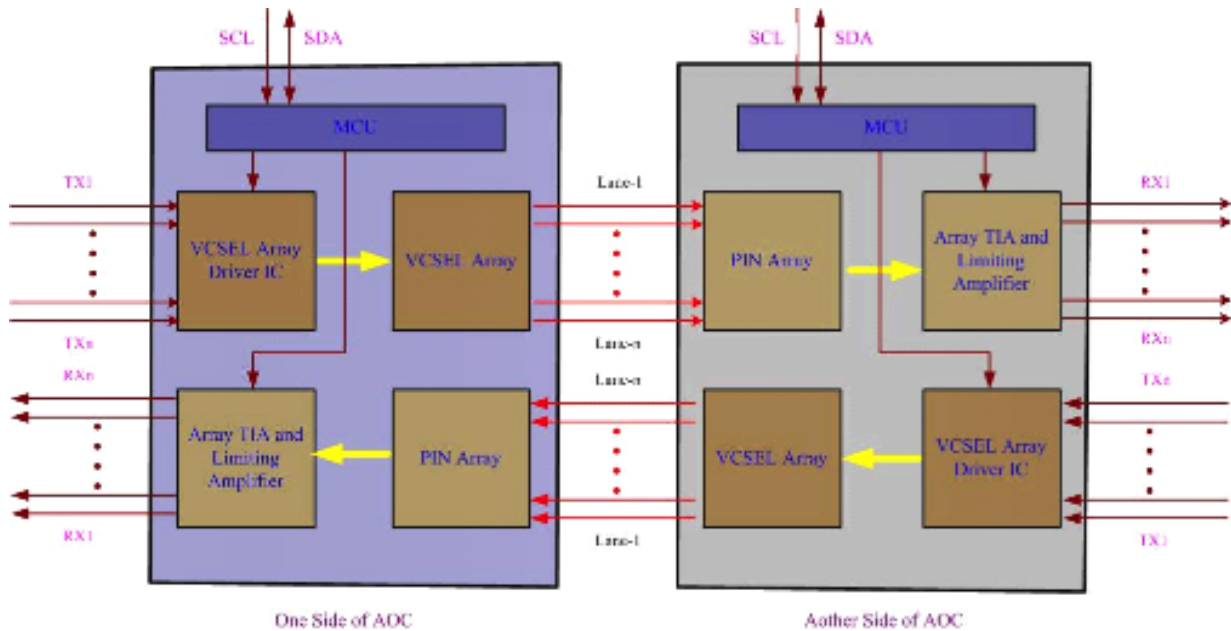
Optical Interface Lanes and Assignment

The optical interface port is a male MPO connector. The four fiber positions on the left as shown below, with the key up, are used for the optical transmit signals (Channel 1 through 4). The fiber positions on the right are used for the optical receive signals (Channel 4 through 1). The central four fibers are physically present.

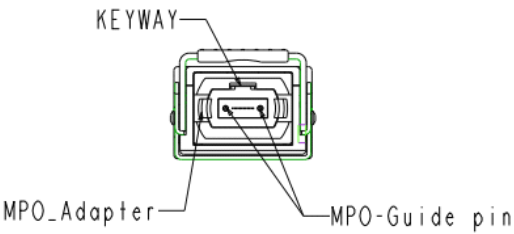
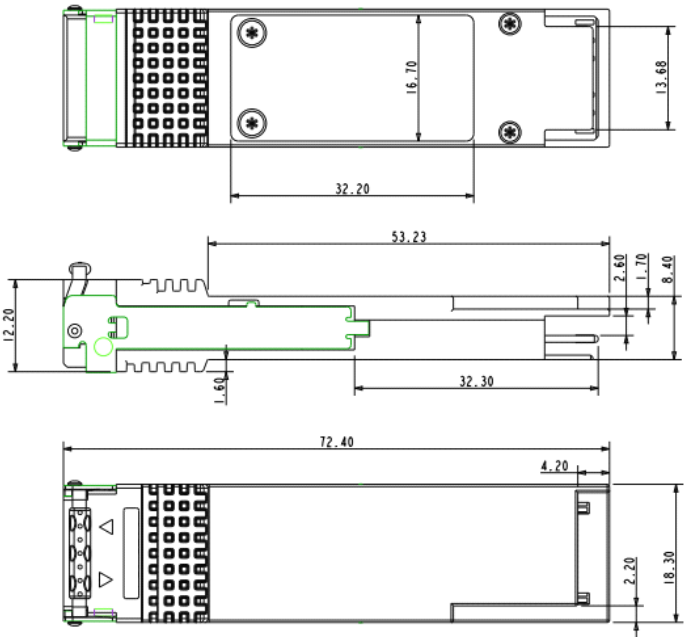


Transmit Channels: 1 2 3 4
Unused positions: x x x x
Receive Channels: 4 3 2 1

Module Block Diagram



Mechanical Specifications



About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is engrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications from ranging from NEBS Level 3 to ISO 9001:2005 with every new development while maintaining the signature reliability of its products.

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